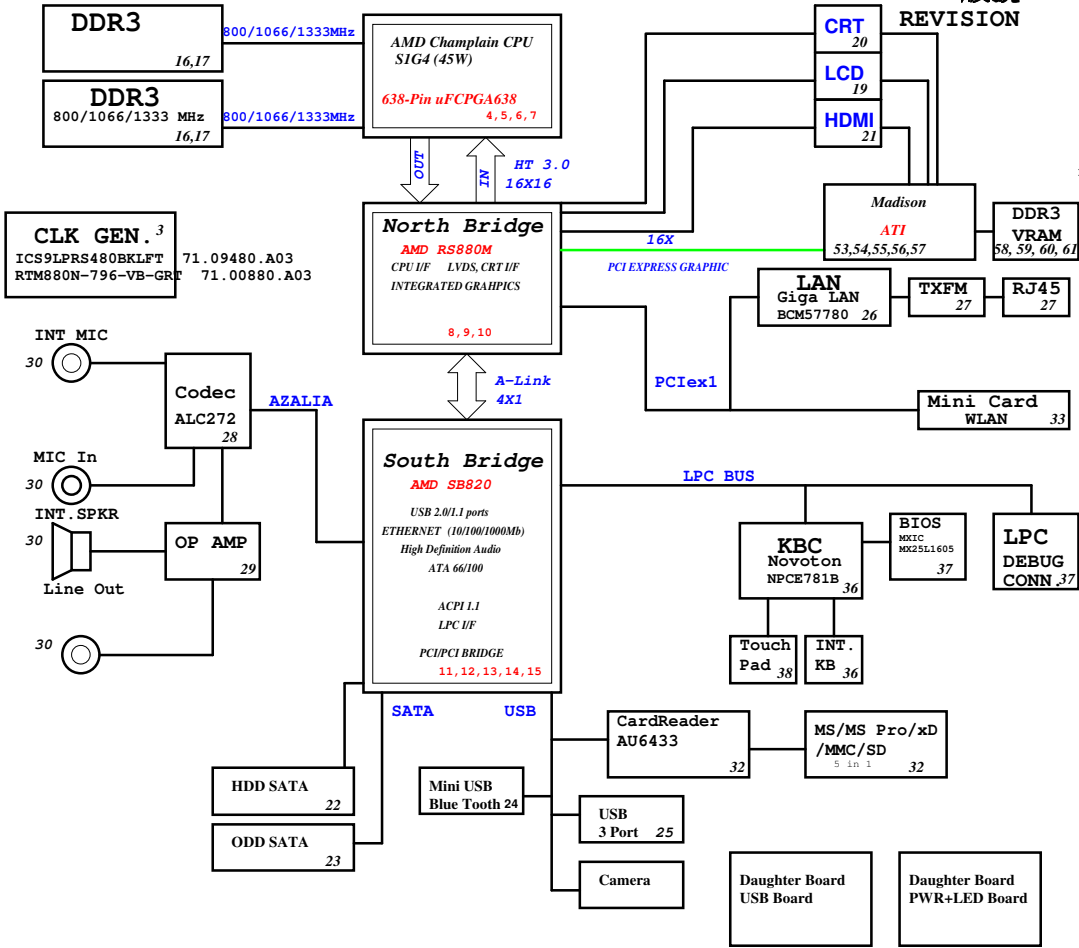


# HM42-DN Block Diagram

Project code: 91.4HD01.001  
PCB P/N : 48.4GX01.0SA  
PCB 版號 : 09919 SA  
REVISION : PCB STACKUP



TOP  
VCC  
S  
S  
GND  
BOTTOM

SYSTEM DC/DC	
RT8223	46
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (5.5A)
	3D3V_S5 (5A)
SYSTEM DC/DC	
RT8209E	47
5V_S5	1D5V_S3 (1.4A)
RT9026	47
5V_S5	OD75_S3 (1.2A)
SYSTEM DC/DC	
RT8209E	48
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0 (11A)
RT9025	48
3D3V_S5	1D1V_S5 (1.4A)
RT9025	49
5V_S5	1D1V_VGA
RT9161	49
3D3V_S0	2D5V_S0 (200mA)
RT9025	49
1D5V_S3	1D05V_S0 (1.4A)
CHARGER	
BQ24745	50
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR
	18V 6.0A
	UP+5V
	5V 100mA
CPU DC/DC	
ISL6265AHR	45
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0
	0~1.55V 18A
	VDDNB
	0~1.55V 4A

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File

BLOCK DIAGRAM

Size

Document Number

JE40-DN

Rev

-3

Date: Friday, March 28, 2010

Sheet 1 of 80

5

4

3

2

1

D

C

B

A

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Title

History

Size

A3

Document Number

JE40-DN

Rev

-3

Date:

Friday, March 28, 2019

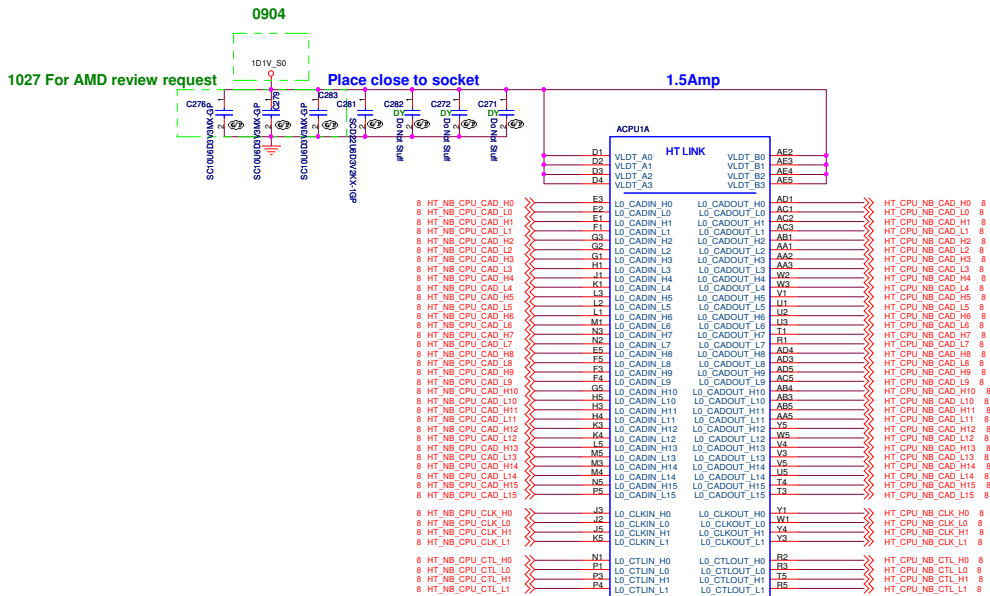
Sheet

2

of

63





SKT-CPU63AP-GP-U2  
62.10055.111  
2ND = 62.10055.181(ENG 未上)

SKT-BGA638H176

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Taipai Hsien 321, Taiwan, R.O.C.

File

CPU HT LINK I/F (1/4)

Rev

A3

Document Number

JE40-DN

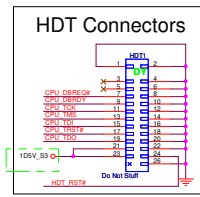
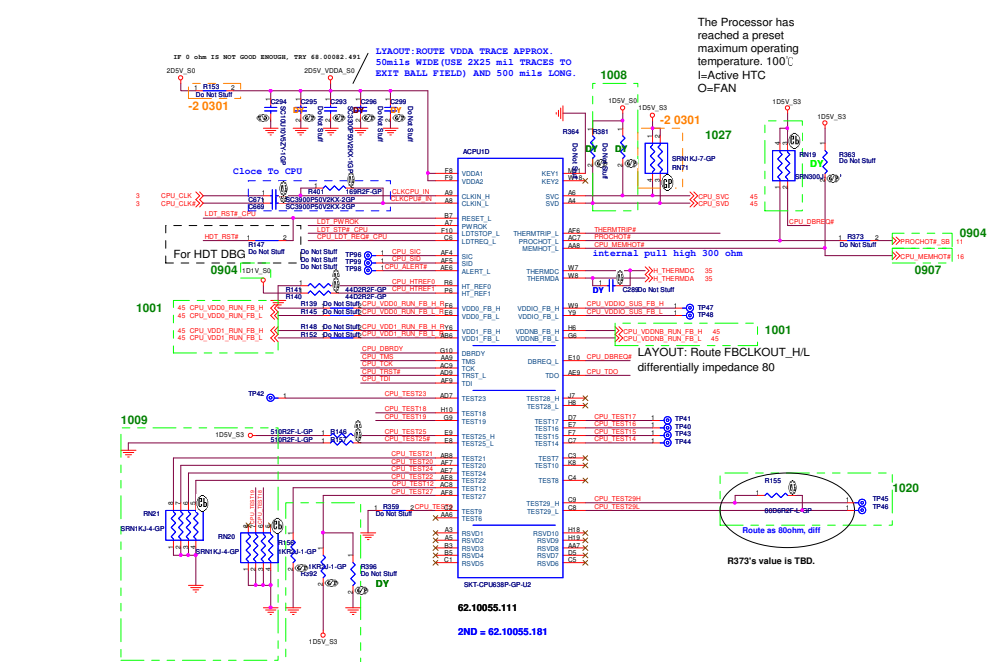
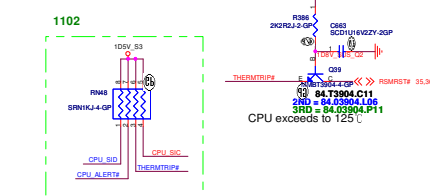
Rev

-3

Date: Friday, March 26, 2010

Sheet 4 of 85





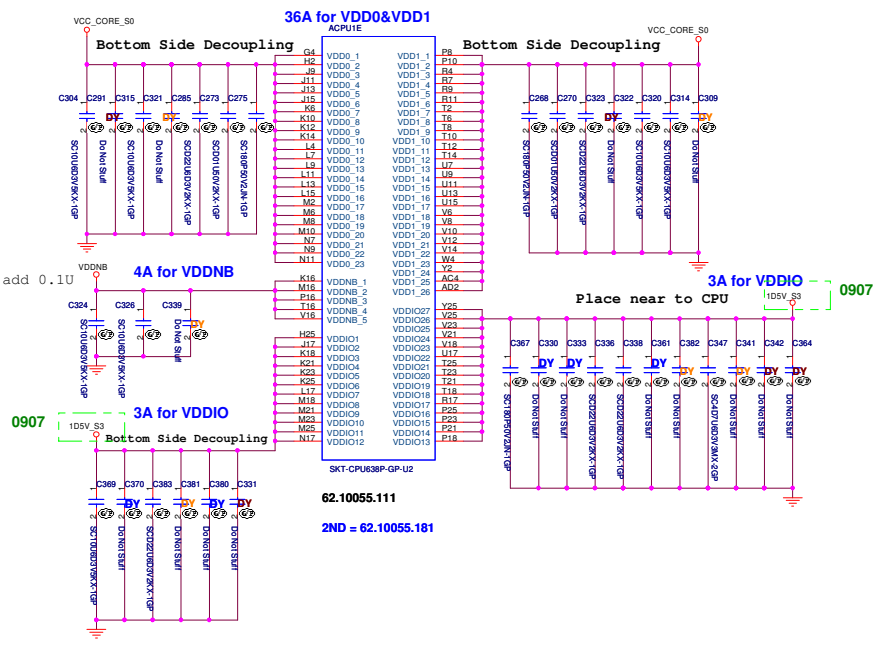
Discrete Madison Hynix			
緯創資通		Wistron Corporation	
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, P.O.C.			
Title CPU_Control&Debug_(3/4)			
Size	Document Number	Rev	
Customs	JE40-DN	-3	
Date: Friday, March 25, 2010		Sheet 6 of	63

ACPU1F		
AA4	VSS1	VSS66
AA11	VSS2	VSS67
AA13	VSS3	VSS68
AA15	VSS4	VSS69
AA17	VSS5	VSS70
AA19	VSS6	VSS71
AB2	VSS7	VSS72
AB7	VSS8	VSS73
AB9	VSS9	VSS74
AB23	VSS10	VSS75
AB25	VSS11	VSS76
AC11	VSS12	VSS77
AC13	VSS13	VSS78
AC17	VSS14	VSS79
AC19	VSS15	VSS80
AC19	VSS16	VSS81
AC21	VSS17	VSS82
AD6	VSS18	VSS83
AD8	VSS19	VSS84
AD25	VSS20	VSS85
AE11	VSS21	VSS86
AE13	VSS22	VSS87
AE15	VSS23	VSS88
AE17	VSS24	VSS89
AE19	VSS25	VSS90
AE21	VSS26	VSS91
AE23	VSS27	VSS92
B4	VSS28	VSS93
B6	VSS29	VSS94
B8	VSS30	VSS95
B9	VSS31	VSS96
B11	VSS32	VSS97
B13	VSS33	VSS98
B15	VSS34	VSS99
B17	VSS35	VSS100
B19	VSS36	VSS101
B21	VSS37	VSS102
B23	VSS38	VSS103
B25	VSS39	VSS104
D6	VSS40	VSS105
D8	VSS41	VSS106
D9	VSS42	VSS107
D11	VSS43	VSS108
D13	VSS44	VSS109
D15	VSS45	VSS110
D17	VSS46	VSS111
D19	VSS47	VSS112
D21	VSS48	VSS113
D23	VSS49	VSS114
D25	VSS50	VSS115
E4	VSS51	VSS116
F2	VSS52	VSS117
F11	VSS53	VSS118
F13	VSS54	VSS119
F15	VSS55	VSS120
F17	VSS56	VSS121
F19	VSS57	VSS122
F21	VSS58	VSS123
F23	VSS59	VSS124
F25	VSS60	VSS125
H7	VSS61	VSS126
H9	VSS62	VSS127
H21	VSS63	VSS128
H23	VSS64	VSS129
JA	VSS65	

SKT-CPU638P-GP-U2

62.10055.111

2ND = 62.10055.181



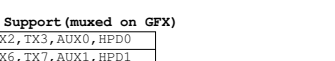
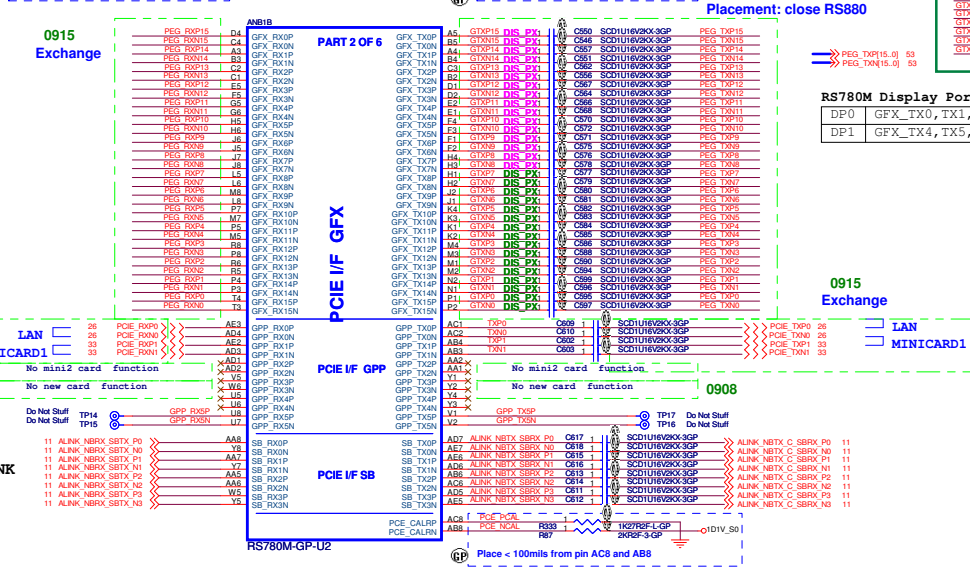
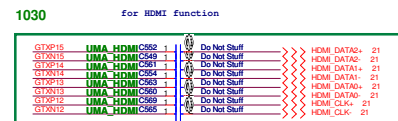
SKT-CPU638P-GP-U2

62.10055.111

2ND = 62.10055.181

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<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
<b>File</b>			
<b>CPU_Power_(4/4)</b>			
<b>Size</b> A3	<b>Document Number</b> <b>JE40-DN</b>	<b>Rev</b> <b>-3</b>	
<b>Date:</b> Friday, March 26, 2010		<b>Sheet</b> 7	<b>of</b> 85







1027 For AMD review request

0.6A per ANT Rev1.1, Page3

0.45A per ANT Rev1.1, Page3

1027 For AMD review request

MEM\_COMP\_P and MEM\_COMP\_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

ANB1F

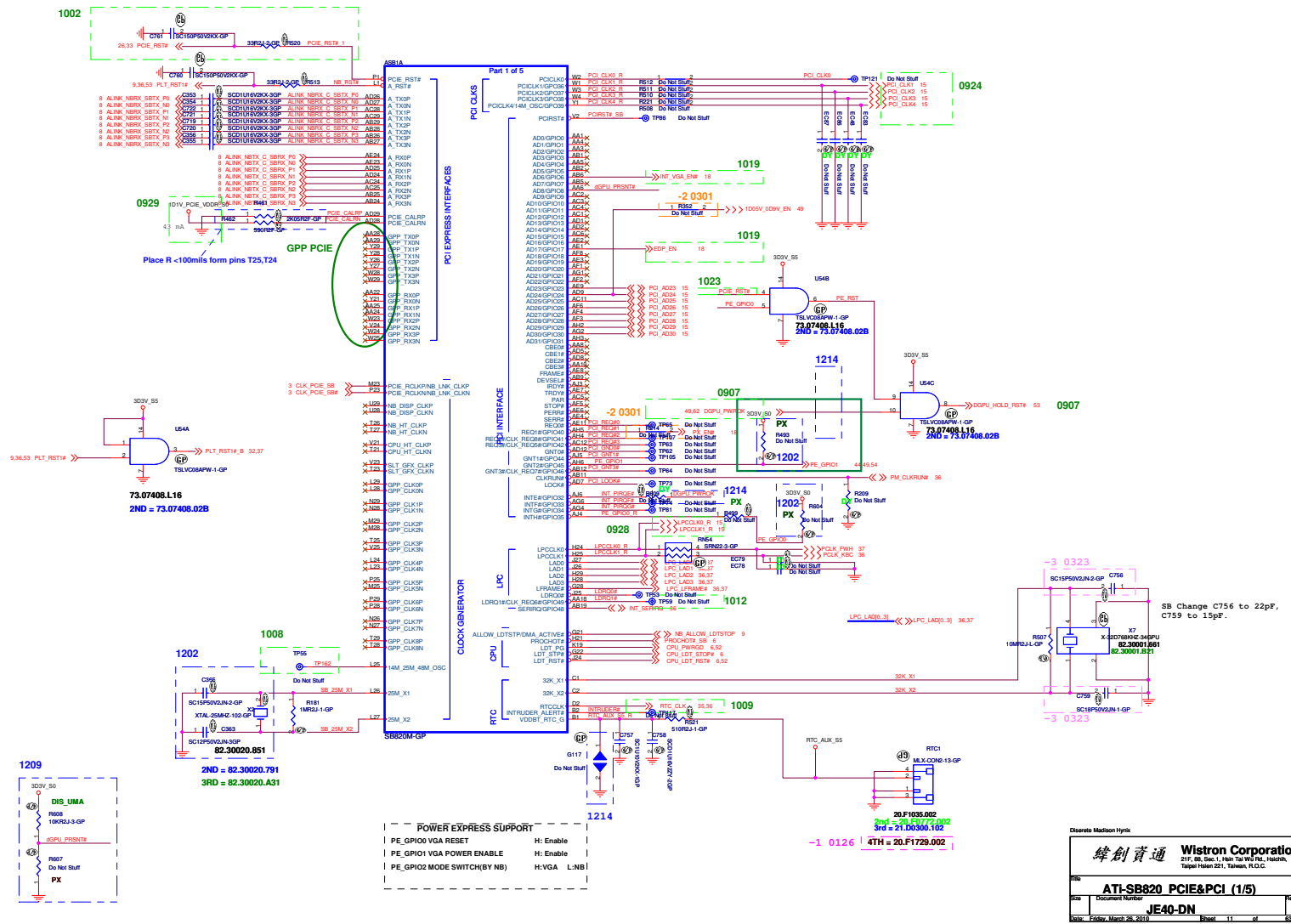
GROUND

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Taipai Hsien 221, Taiwan, R.O.C.

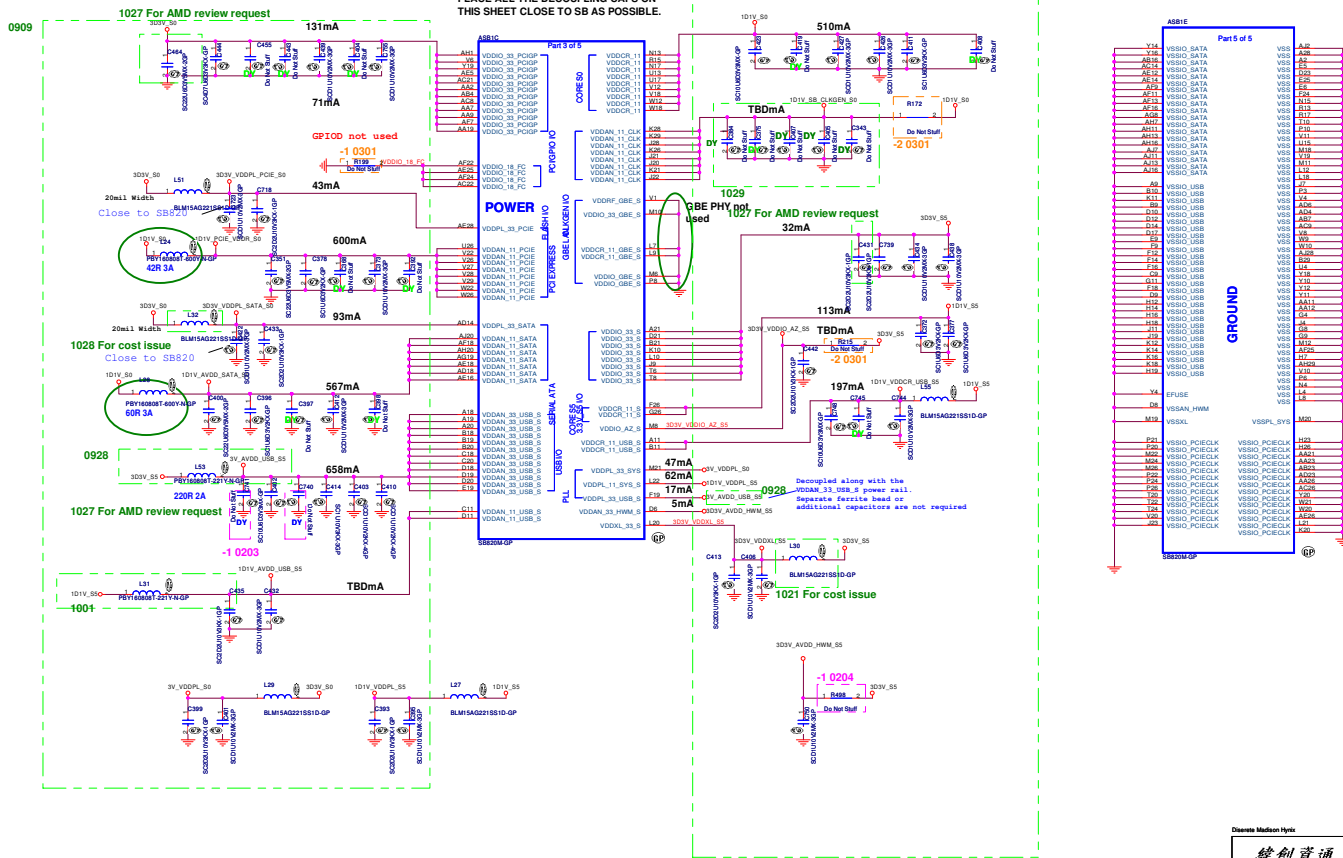
File  
AT1-RS880M\_Side Port&PWR&GND(3/3)  
Doc  
Document Number  
JE40-DN  
Date: Friday, March 26, 2010  
Sheet 10 of 30





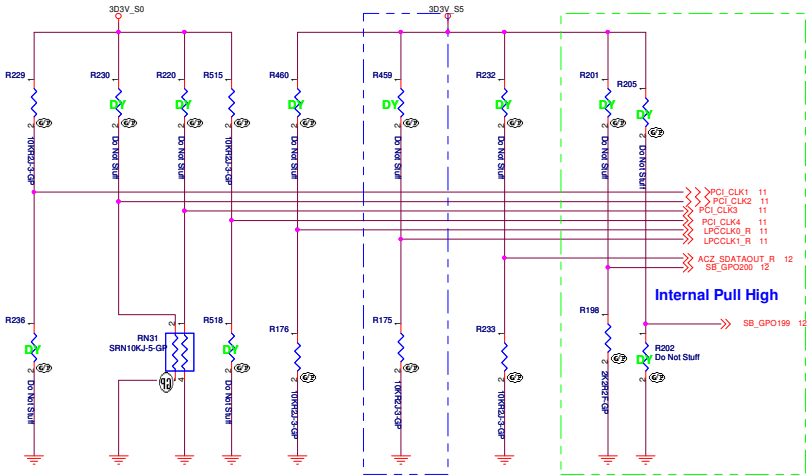
Title			
<b>ATI-SB820 SATA-IDE (3/5)</b>			
Size	Document Number	Rev	
<b>A3</b>	<b>JE40-DN</b>	<b>-3</b>	
Date:	Friday, March 26, 2010	Sheet	13 of 63

PLACE ALL THE DECOUPLING CAPS ON  
THIS SHEET CLOSE TO SB AS POSSIBLE.



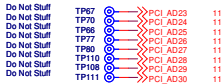
REQUIRED SYSTEM STRAPS

1115



1002

DEBUG STRAPS



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCIe Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved L,L = SPI ROM	
PULL LOW	FORCE PCIe Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FW ROM	

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

Discrete Madison Hybrid

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Title

ATI-SB820 STRAPPING (5/5)

Size

A3

Document Number

JE40-DN

Rev

-3

Date

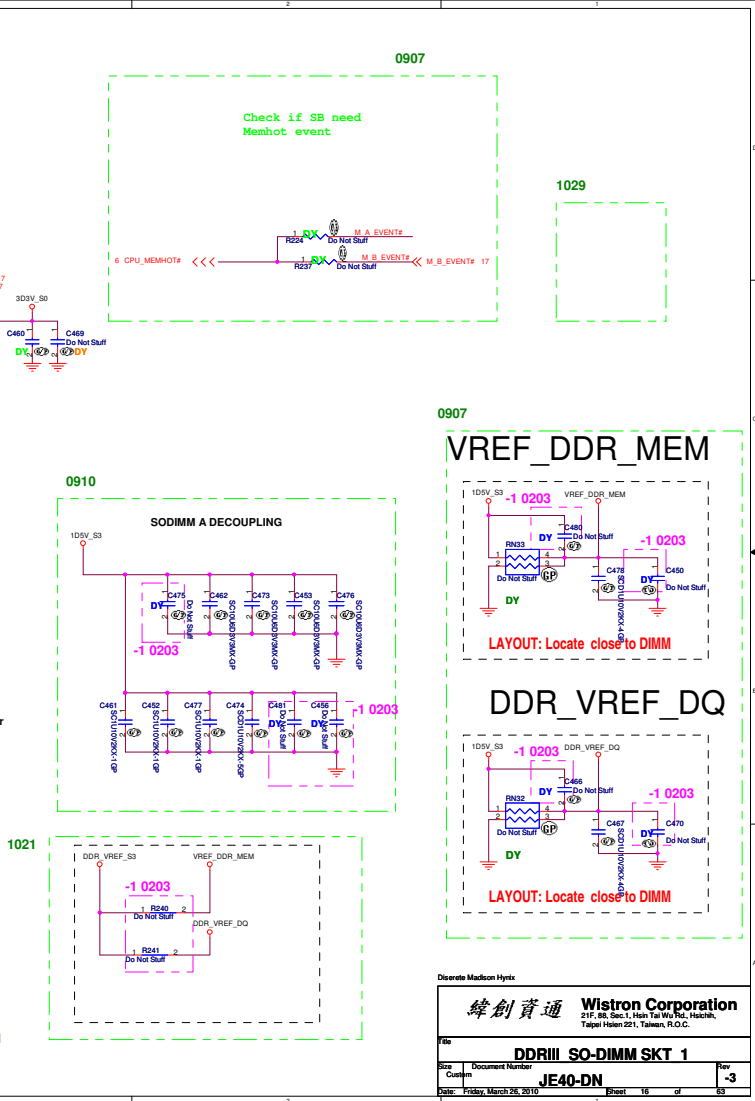
Friday, March 26, 2010

Sheet

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of

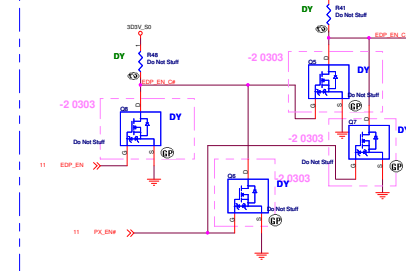
83







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File			
		<b>DDRIII SO-DIMM SKT 2</b>	
Size	Document Number		Rev
Custom	<b>JE40-DN</b>		<b>-3</b>
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Truth Table

Function	SEL
A <sub>N</sub> to B <sub>1</sub>	L
A <sub>N</sub> to B <sub>2</sub>	H

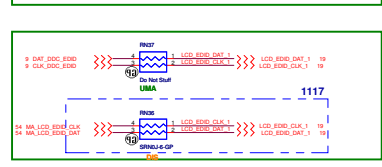
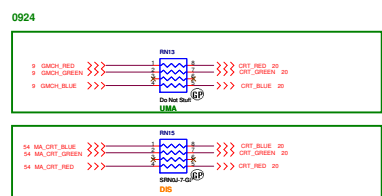
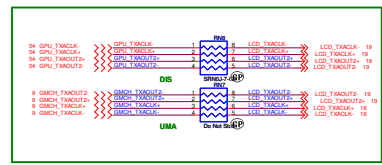
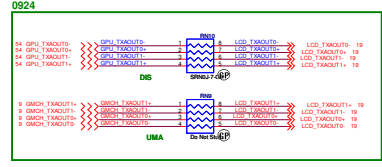
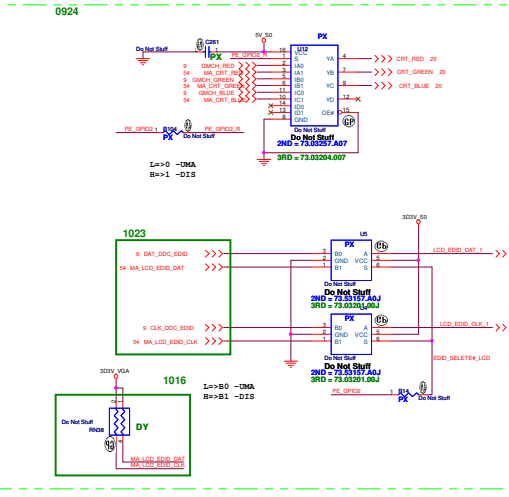
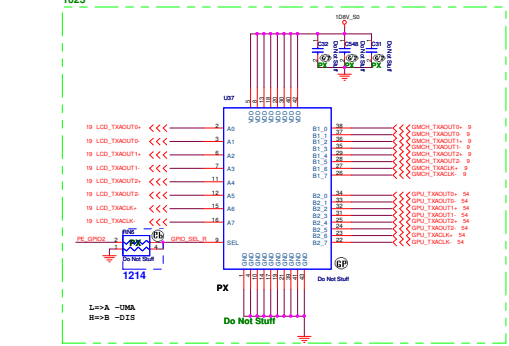
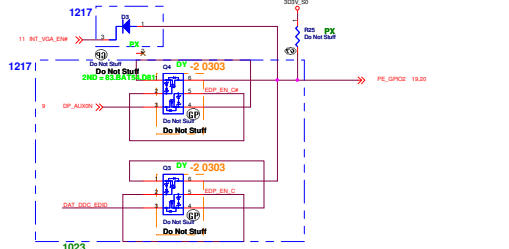
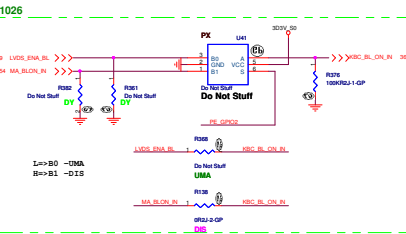
E	S	YA	YB	YC	YD	Function
H	X	Hb-Z	Hb-Z	Hb-Z	Hb-Z	Disable
L	L	IA0	IB0	IC0	ID0	S=0
L	H	IA1	IB1	IC1	ID1	S=1

Function Table

Input (B)	Function
L	E <sub>1</sub> Connected to A
H	E <sub>1</sub> Connected to B

Function Table

Input (B)	Function
L	E <sub>1</sub> Connected to A
H	E <sub>1</sub> Connected to B



[illegible]

CCD Pin	
Pin	Symbol
1	CCD_PWD
2	USB-
3	USB+
4	GND
5	GND

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[illegible]

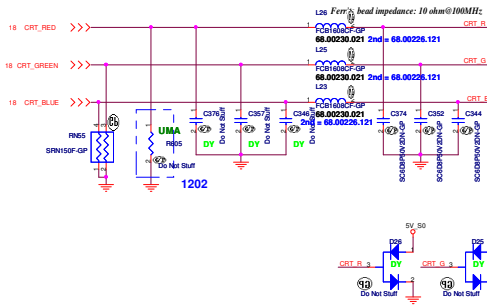
Size	Document Number
Custom	JE40-DN

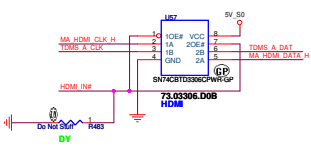
Date: Friday, March 26, 2010

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Flow

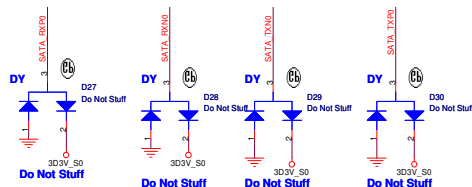
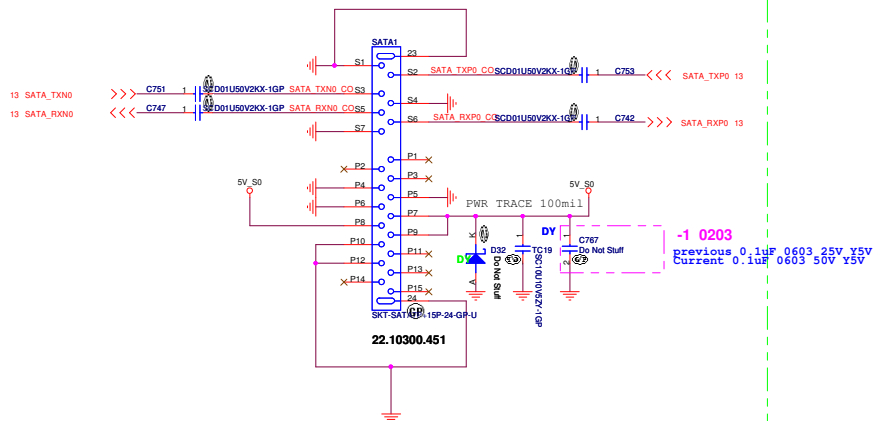
Design Rule  
Place these annotations  
close to the CRT-conn  
connection





# SATA Connector

0923



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Taipai Hsien 221, Taiwan, R.O.C.

File

**HDD**

Size

Document Number

**JE40-DN**

Rev

**-3**

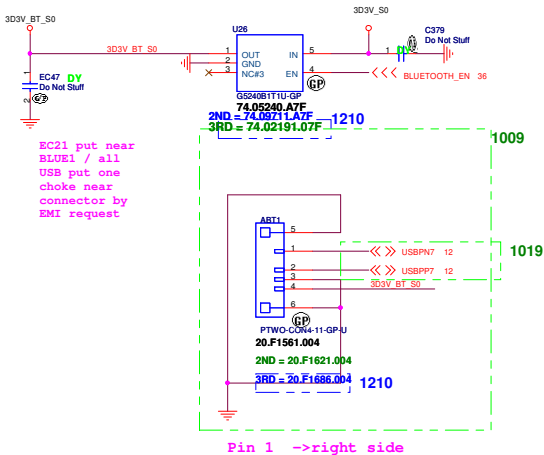
Date: Friday, March 26, 2010

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# BLUETOOTH MODULE

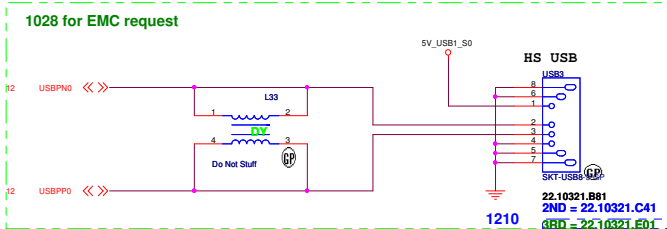
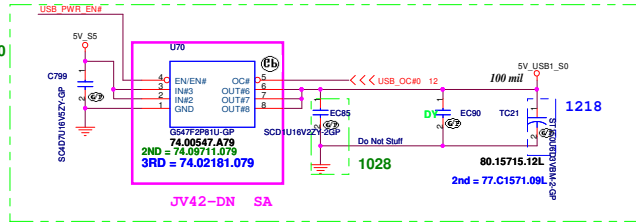
1.5A / High Active Voltage 2V



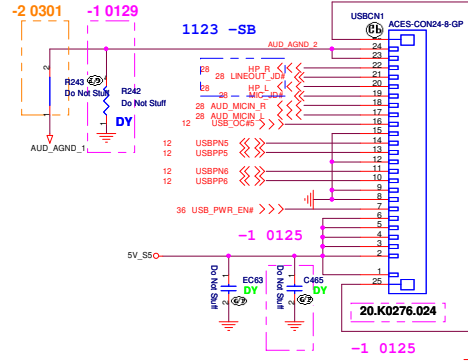
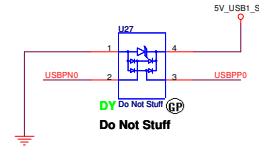
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Title			
<b>BLUETOOTH</b>			
Size	Document Number		Rev
	<b>JE40-DN</b>		<b>-3</b>
Date:	Friday, March 26, 2010	Sheet 24 of	63





Pin1 -> right side  
 22.10218.T51 Pin1 -> left side (JV42-DN)  
 change Net sequence



Eng stuff 20.K0216.024 Pin1 -> left side  
 PD change to 20.K0276.024 Pin1 -> left side  
 so do not swap net



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File

Size Document Number

USB

JE40-DN

Date: Friday, March 28, 2019

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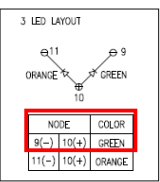
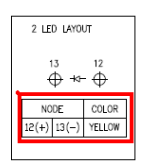
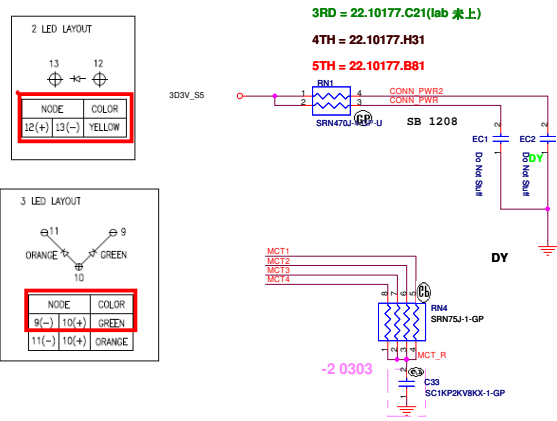
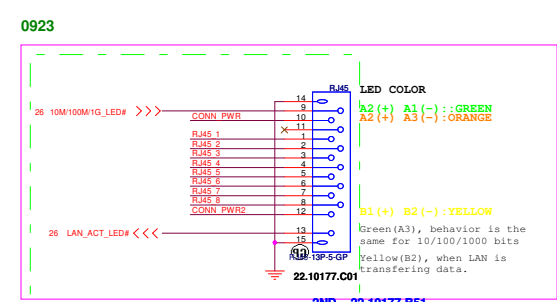
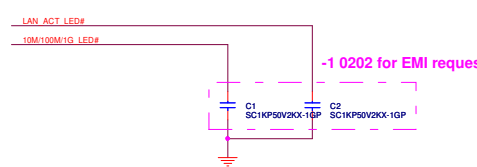
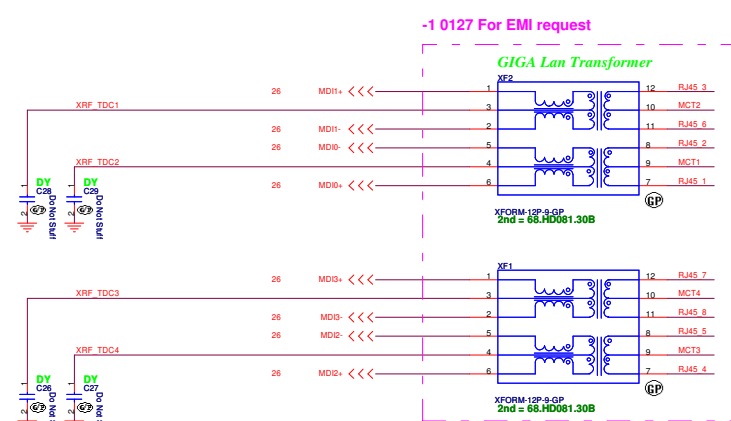
Rev -3



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

LAN Connector



Discrete Madison Hynix

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File

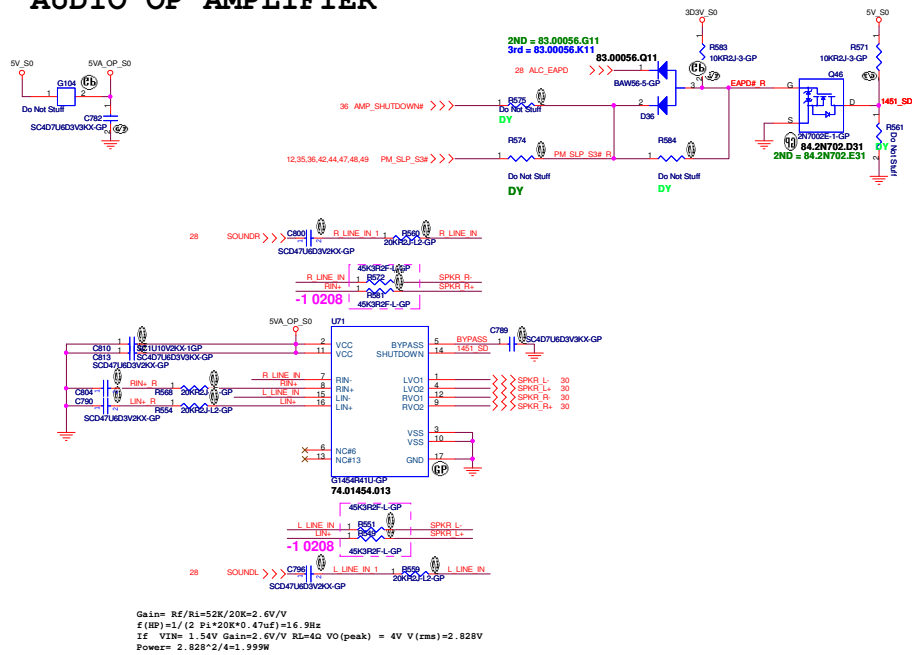
LAN CONN

Size A3 Document Number JE40-DN Rev -3

Date: Friday, March 28, 2019 Sheet 27 of 30



AUDIO OP AMPLIFIER



Discrete Madison Hynix

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Taipei Hsien 221, Taiwan, R.O.C.

Rev

**AUDIO AMP**

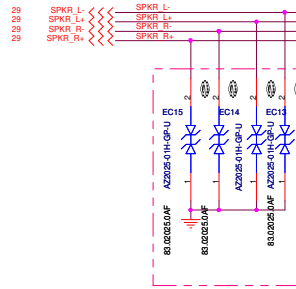
**JE40-DN**

Doc No: Friday, March 26, 2010 Sheet 29 of 63 Rev -3

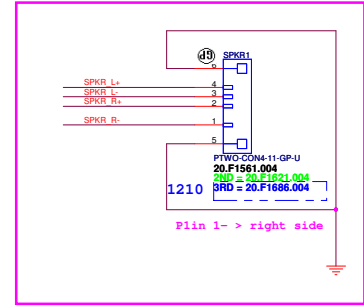
# Internal Speaker

0914

0910



-1 0125 for EMI request



Pin 1 -> right side

JV42-DN SA

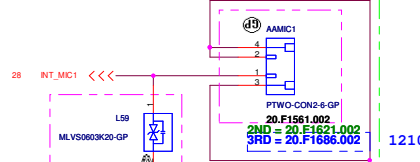
0910

## LINE OUT

0911

1016

## Internal Mic



-1 0209 For MIC issue

JV42-DN PX

Pin 1- >right side

20.F1240.002 Pin1->left side

same as JV70-CP

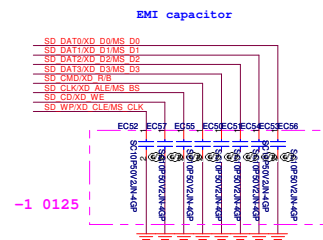
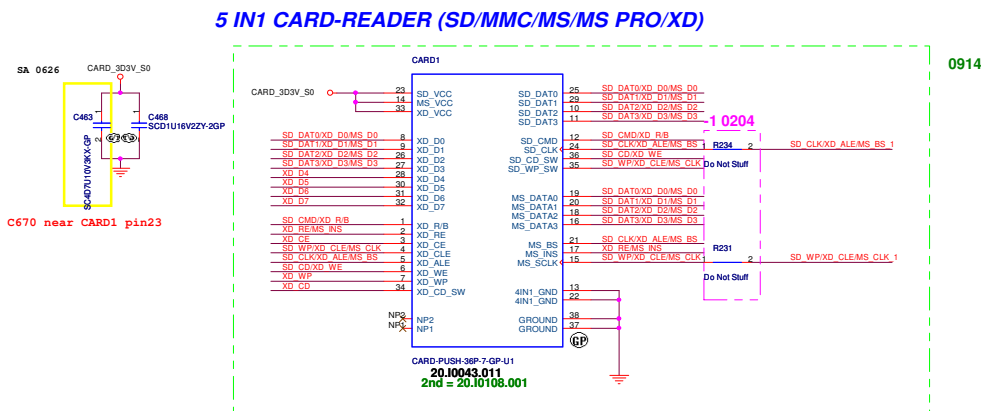
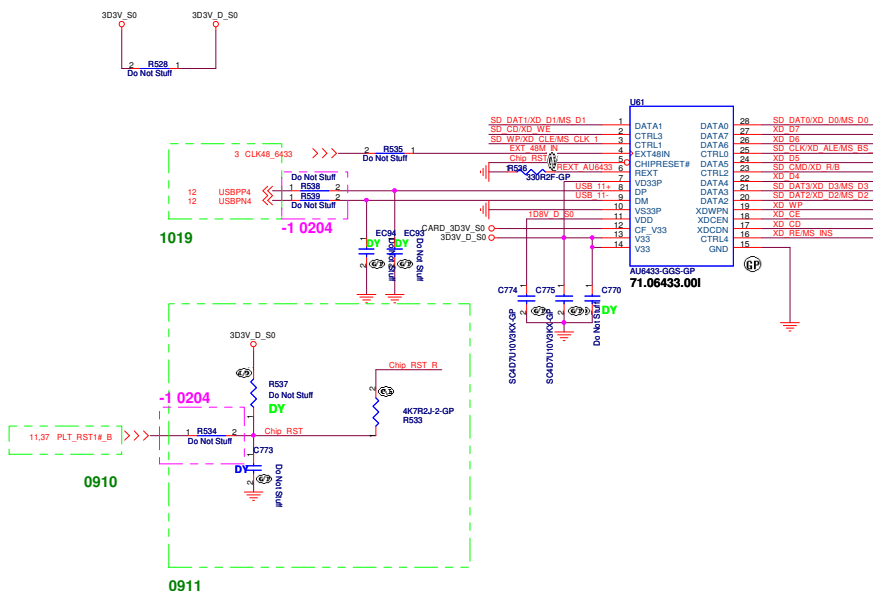
Discrete Madison Hynd

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.		File	
<b>AUDIO JACK</b>		Size	
<b>JE40-DN</b>		Document Number	
Date: Friday, March 28, 2019		Rev	
Sheet 30 of 63		-3	

No Modem Function

Discrete Madison Hynix

緯創資通		Wistron Corporation	
		21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		MDC	
Size	Document Number		Rev
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Date: Friday, March 26, 2010		Sheet	31 of 63



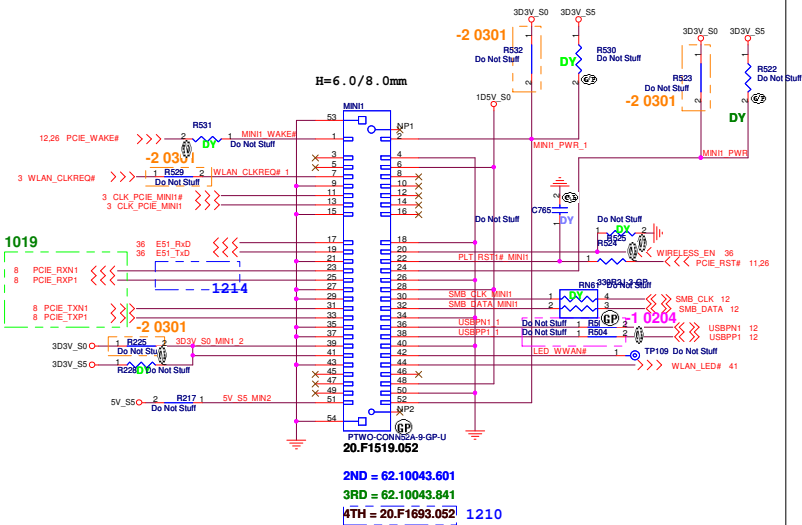
Discrete Madison Hynix

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

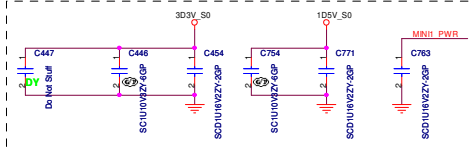
Title			
<b>CARDREADER</b>			
Size	Document Number	Rev	
	<b>JE40-DN</b>	<b>-3</b>	
Date:	Friday, March 26, 2010	Sheet	32 of 63



0923



Place near MINI1



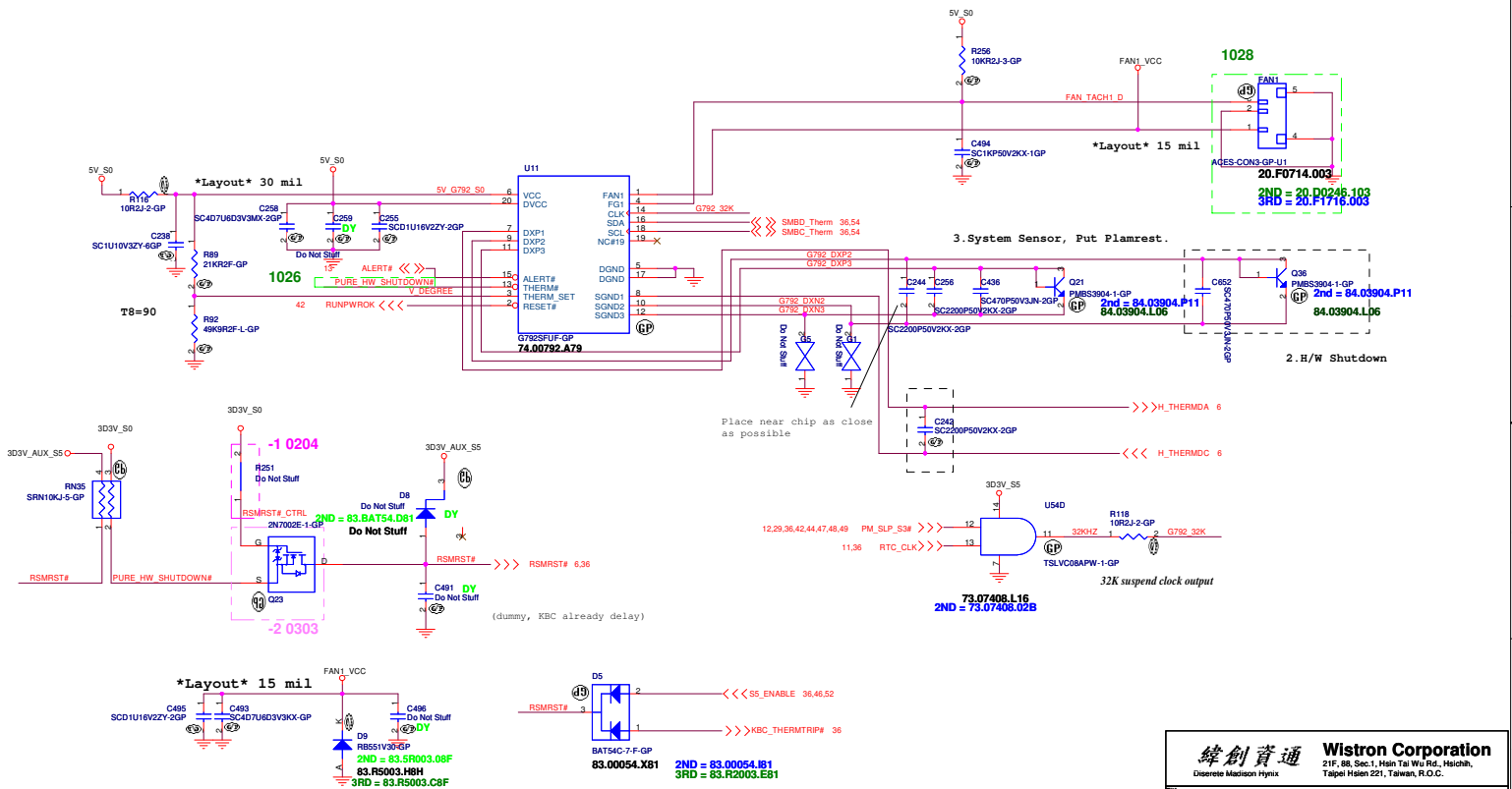
### *No Mini Card Function (Robson2 and 3G)*

Discrete Madison Hynix		<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>MINI CARD</b>			
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No NEWCARD Function

Discrete Madison Hyinx

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		21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taippei Hsien 221, Taiwan, R.O.C.	
File			
NEW CARD			
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Title			
		<b>G792</b>	
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for ENE FAE suggest, SPICS# is push-pull pin,  
don't need to pull high

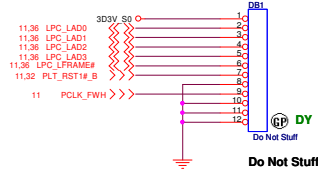
base on FAE Kevin discuss with KBC

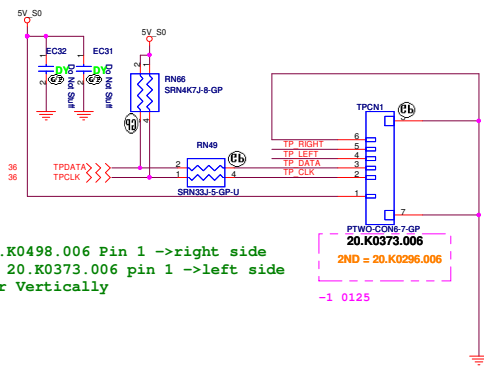
-1 0205  
-2 0303

3rd 4th source LAB ENG未上  
16M Bits  
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD

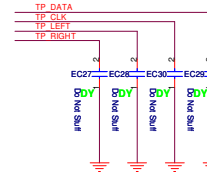
11.36 LPC\_LAD[0..3] <<> LPC\_LAD[0..3]



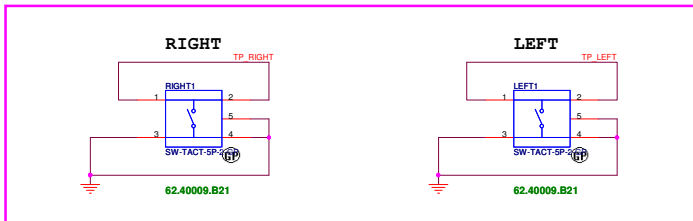


Eng stuff 20.K0498.006 Pin 1 -->right side  
 PD change to 20.K0373.006 pin 1 -->left side  
 so net mirror Vertically

PTWO-CONA-7-GP  
 20.K0373.006  
 2ND = 20.K0296.006  
 -1 0125



-1 0205



No Finger printer Function

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Title

**Touch PAD**

Size

Document Number

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NONE BOARD

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NONE BOARD			
Size	Document Number		Rev
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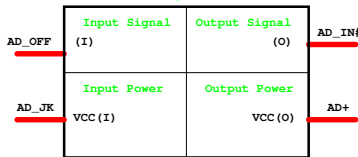




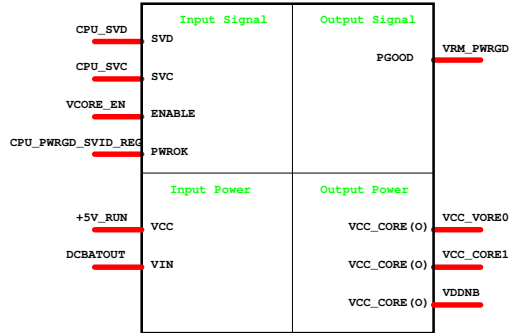




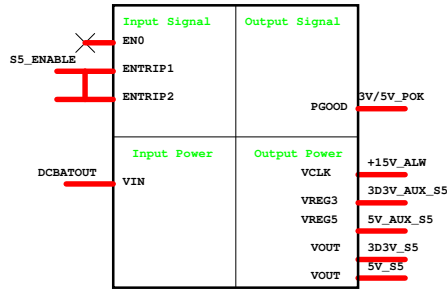
### Adapter



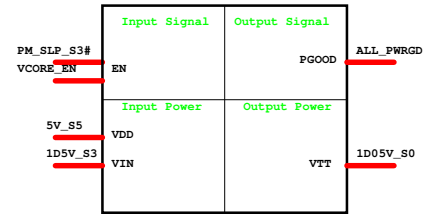
### CPU\_CORE ISL6265HRTZ



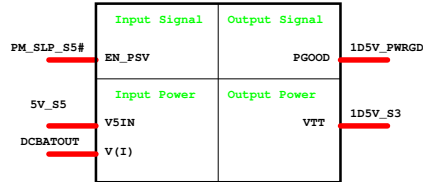
### DCDC 5V/3D3V(RT8223)



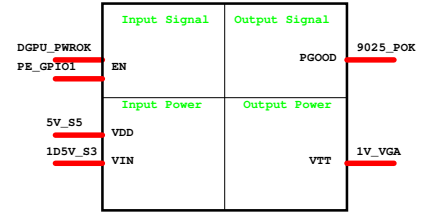
### DCDC 1D05V\_S0(RT9025)



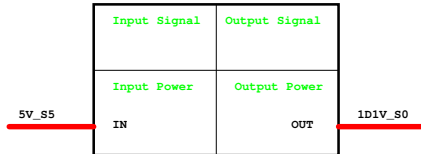
### DCDC 1D5V(RT8209E)



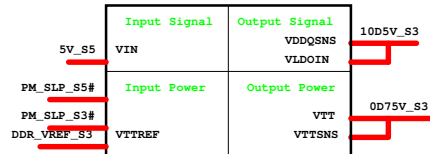
### DCDC 1V\_VGA(RT9025)



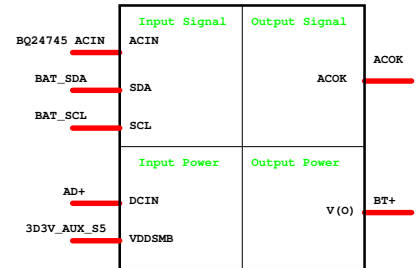
### 1D1V LDO RT8209E



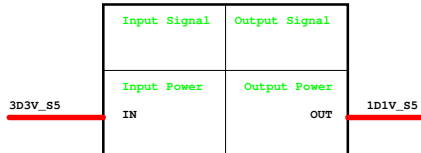
### 0D75V LDO RT9026



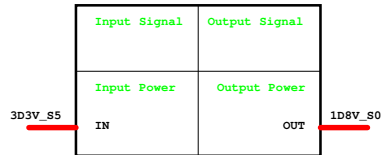
### CHARGER BQ24745



### 1D1V LDO RT9025



### 1D8V LDO RT8015A



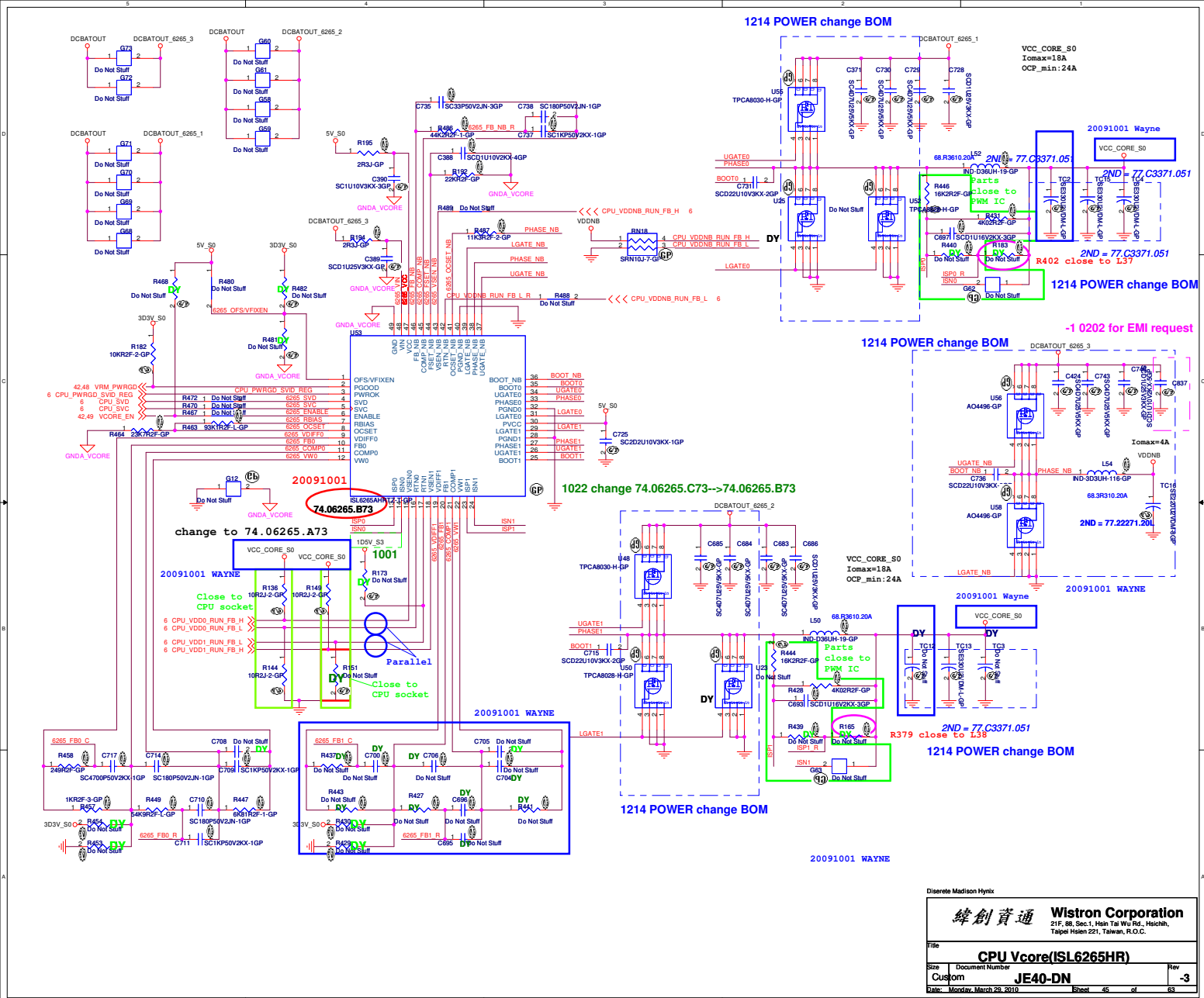
Discrete Madison Hynix

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Power Block Diagram		
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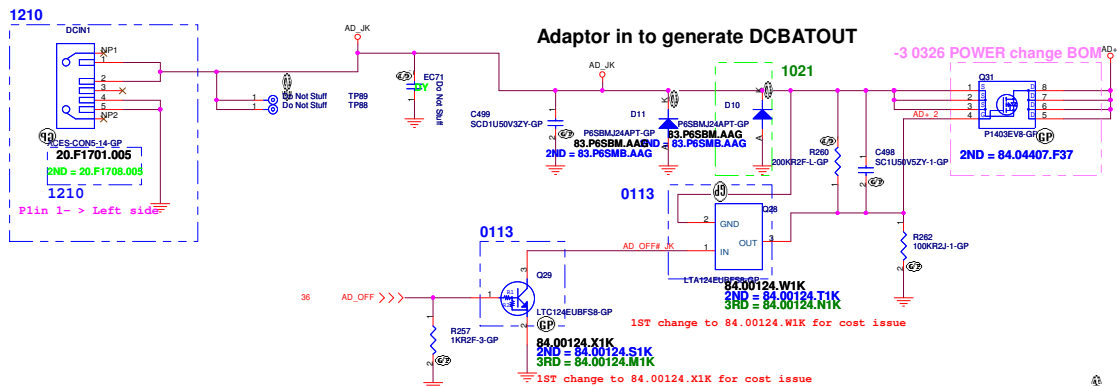


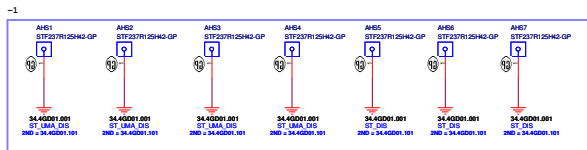
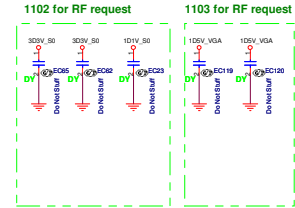
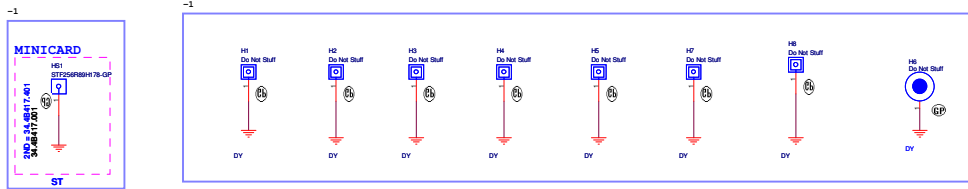
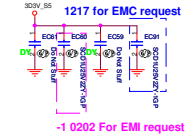








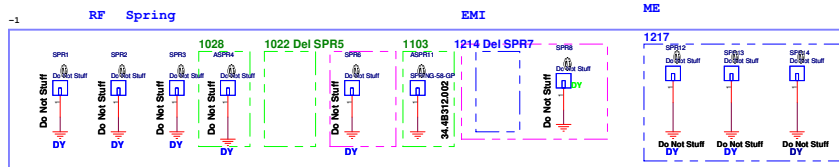




**Check test point**



Test Point放在Dimm Door打開可量測處



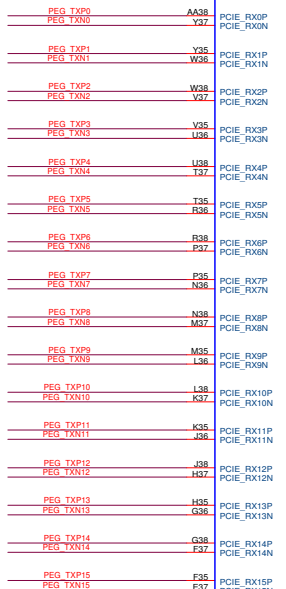
Discrete Madson Hyrax

緯創資通

**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

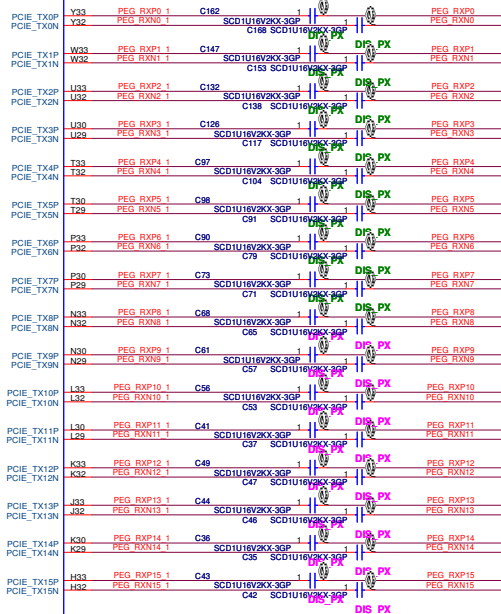
File			EMI/Spring/Boss		
Size	Document Number				Rev
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8 PEG\_TXP[15:0] << PEG\_TXP[15:0]  
8 PEG\_TXN[15:0] << PEG\_TXN[15:0]

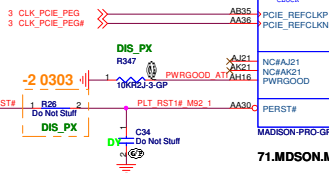


PCI EXPRESS INTERFACE

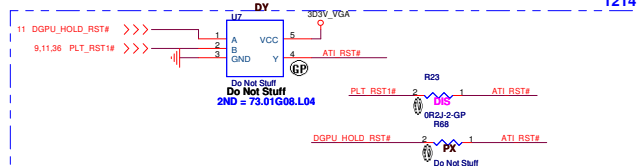
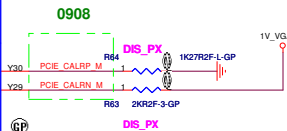
1 OF 8



8 PEG\_RXP[15:0] << PEG\_RXP[15:0]  
8 PEG\_RXN[15:0] << PEG\_RXN[15:0]



CALIBRATION  
PCIE\_CALRP  
PCIE\_CALRN



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Title	
Madison PCIE	
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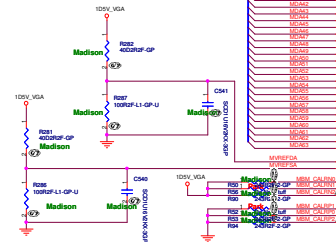




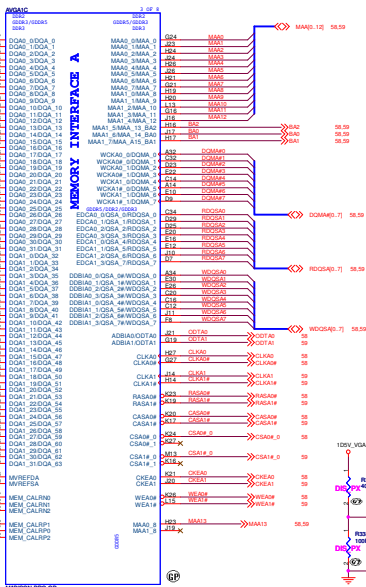


For SSTL-1.8/SSTL-2/DRL/GDR1: 0.5 \* VDDR1.  
For DOR3/GDR3/GDR4/GDR5: 0.7 \* VDDR1.

DIVIDER RESISTORS	GDR5	DOR3	DOR3
MYREF	1.5V	1.8/1.5V	1.5V
MYREF TO PWR	40.2K	50.2K	40.2K
MYREF TO GND	100K	100K	100K



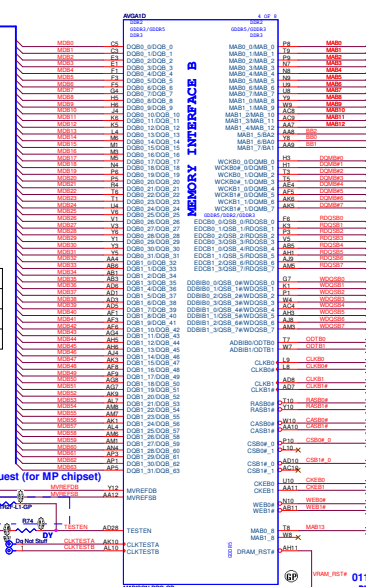
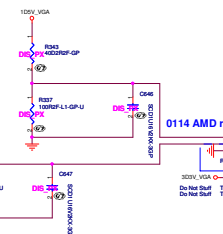
Madison: MEM\_CALRP[0,2] signals are used  
Park: MEM\_CALRP1 and MEM\_CALRP1 are used



71.MDS0N.M01  
Madison->71.MDS0N.M01, Park->71.GPARK.M04

For SSTL-1.8/SSTL-2/DRL/GDR1: 0.5 \* VDDR1.  
For GDR3/GDR3/GDR4/GDR5: 0.7 \* VDDR1.

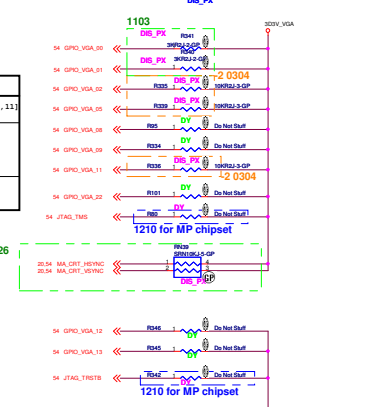
DIVIDER RESISTORS	GDR5	DOR3	DOR3
MYREF	1.5V	1.8/1.5V	1.5V
MYREF TO PWR	40.2K	50.2K	40.2K
MYREF TO GND	100K	100K	100K



71.MDS0N.M01  
Madison->71.MDS0N.M01, Park->71.GPARK.M04

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS S: DO NOT RETAIL RESISTOR 1: RETAIL RESISTOR X: DESIGN DEPENDENT NA: NOT APPLICABLE
TX_PWRN_ENB (Internal PD)	GP100	FOR FULL TX OUTPUT SWING Transmitter Power Savings Enable = 50k Tx output swing = Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GP101	Transmitter De-emphasis Enable = 0: 2x de-emphasis disabled = 1: 2x de-emphasis enabled	X
RESERVED	GP108	RESERVED	0
BIF_VGA_DIS	GP109	VGA ENABLED	0
RESERVED	GP1021	RESERVED	0
BIOS_ROM_EN	GP1022_ROMCS	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GP10[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT If BIOS_ROM_EN=1, then Config[3:0] Defines the ROM type If BIOS_ROM_EN=0, then Config[3:0] Defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	R2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 0:No audio function 1:Audio for DisplayPort and HDMI (1 if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

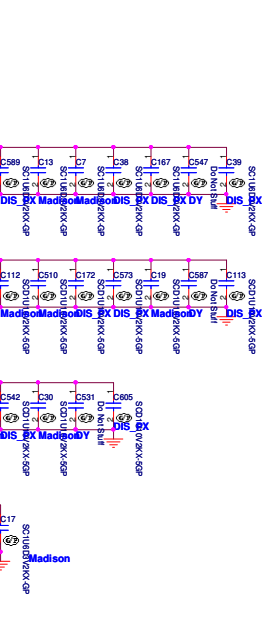
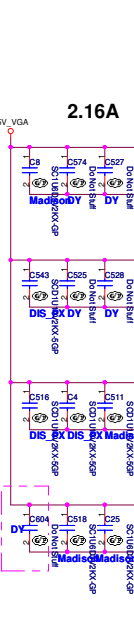
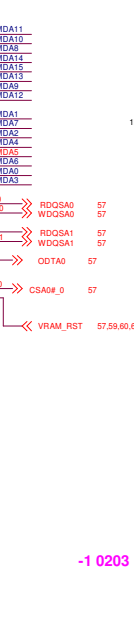
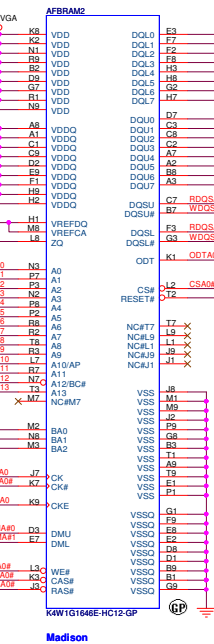
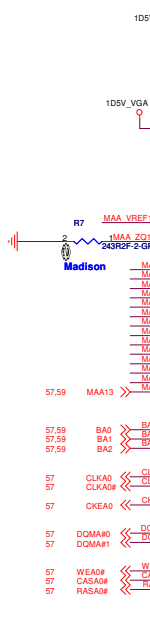
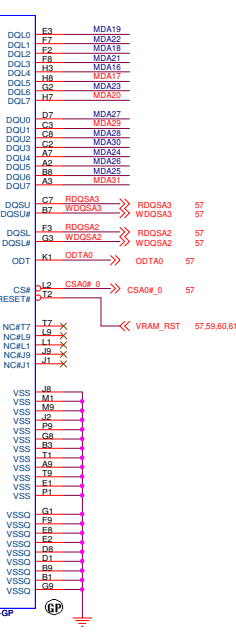
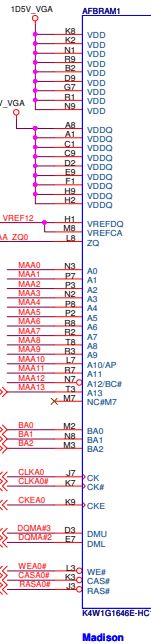
AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLED PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
R2SYNC, GENERRIC, GPIO2, GPIO21			
If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory aperture	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	ST	M25P05A
256MB	x001	Microelectronics	M25P10A
512MB	x010		M25P20
1GB	x011		M25P40
2GB	x012		M25P80
4GB	x013		M25P16A
		Chingis (Formerly PMC)	Ph25LV01A



Designator	For M97-M2	For Mannheim
R_MEM_1	10K	10K
R_MEM_2	40K/Short	51K
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

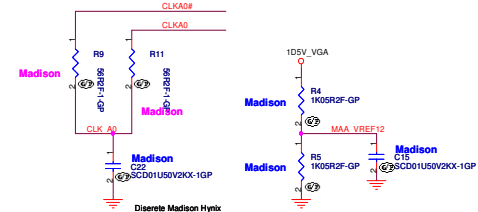
Wistron Corporation  
217 St. Louis, 11th Floor, Wistron, Taipei 10611, Taiwan, R.O.C.  
Madison Memory / Straps  
JE40-DN  
3

# DDR3



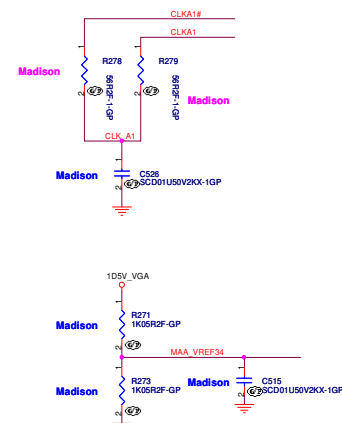
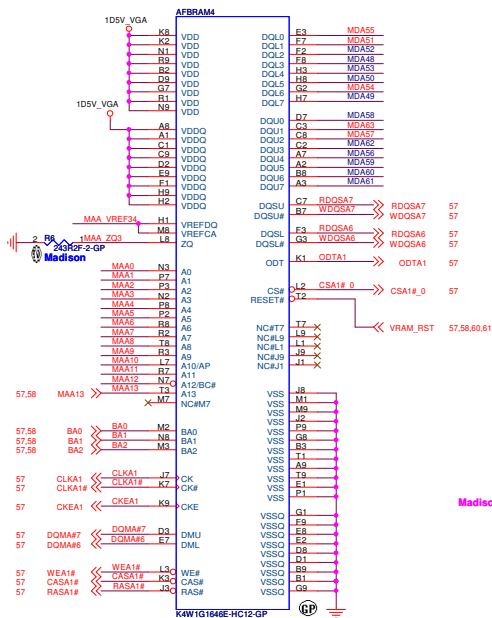
SAMSUNG: 72.41164.H0U  
HYNIX: 72.51G63.C0U

57.59 DQMA#(0..7) <<>  
57.59 RDQSA(0..7) <<>  
57.59 WDQSA(0..7) <<>  
57.59 MAA(0..12) <<>  
57.59 MDA(0..63) <<>



File		Wistron Corporation	
Size		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi, Taipei Hsin 221, Taiwan, R.O.C.	
Date		Friday, March 28, 2010	
Document Number		JE40-DN	
Rev		3	

2.41164.H0U  
2.51G63.C0U

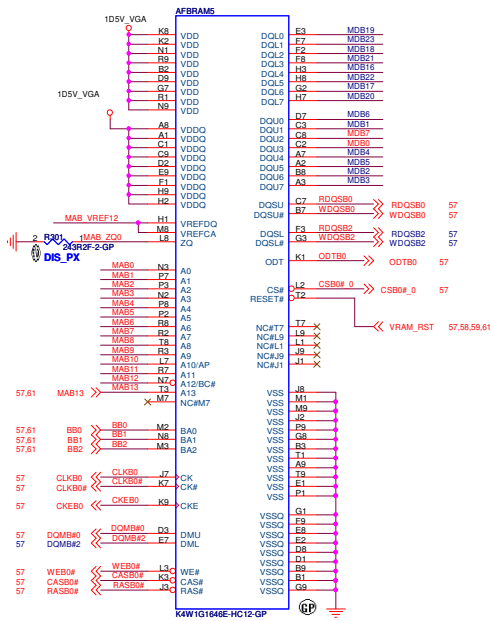


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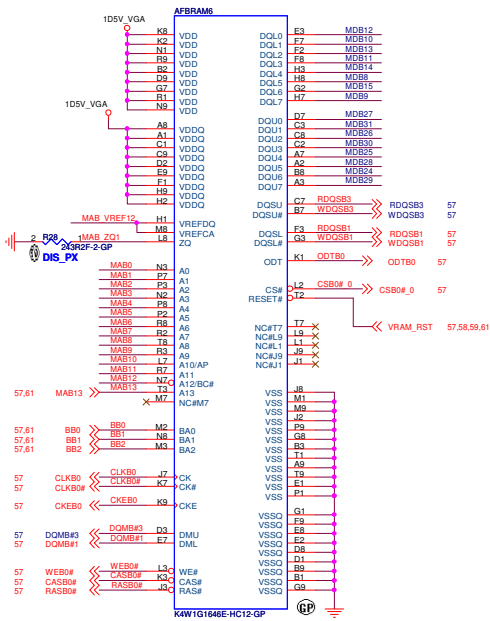
Title			
<b>VRAM(2/4)</b>			
Size A3	Document Number		Rev -3
<b>JE40-DN</b>			
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# DDR3

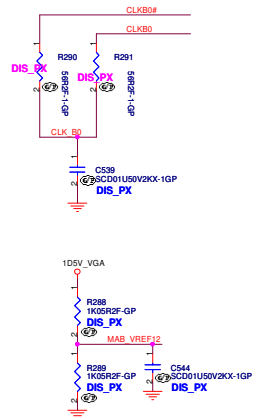


72.41164.H0U

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SAMSUNG: 72.41164.H0U
HYNIX:   72.51G63.C0U
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72.41164.HOU



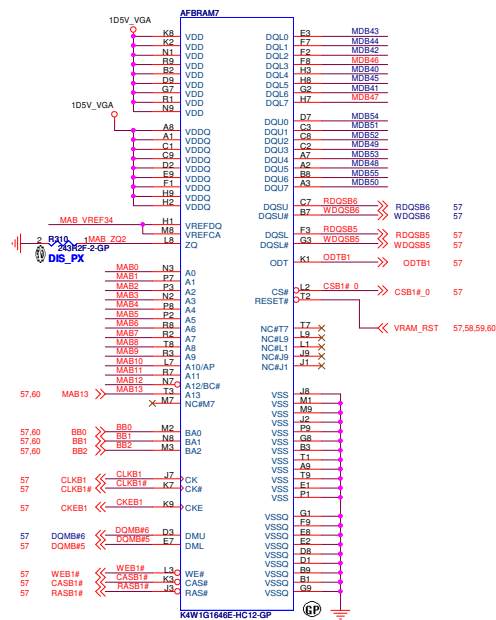
Discrete Madison Hynix

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
VRAM(3/4)			
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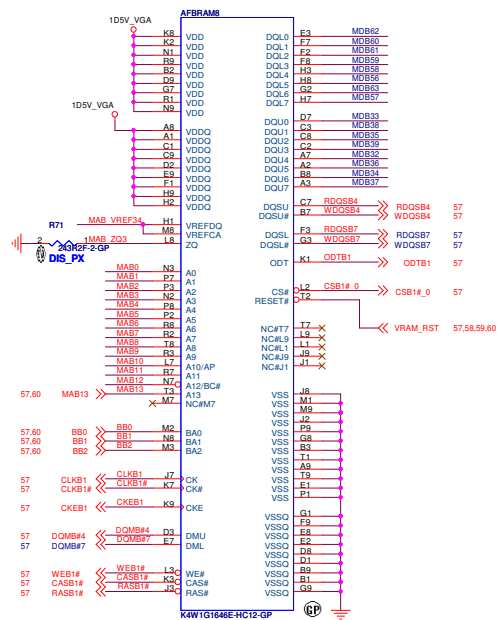
## DDR3



DIS PX

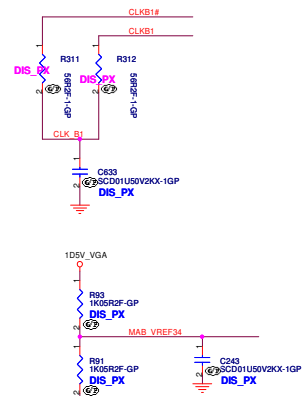
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SAMSUNG: 72.41164.H0U  
HYNIX: 72.51G63.C0U



DIS\_PX

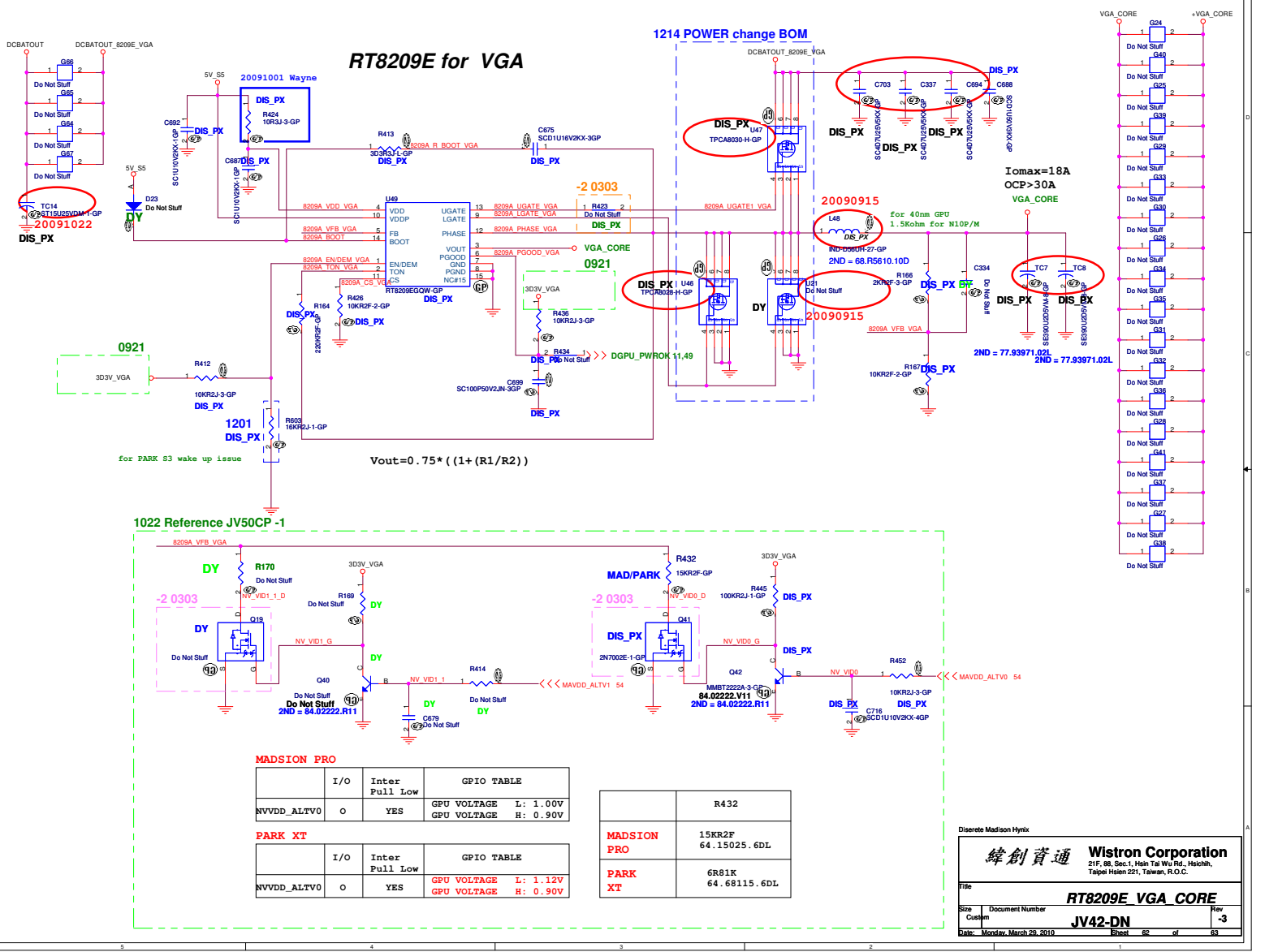
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Title			
<b>VRAM(4/4)</b>			
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Discrete Madison Hynix

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Title

NOTE

Size A3

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Date: Monday, March 29, 2010

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